**UNIVERSIDAD TECNOLÓGICA DE QUERÉTARO**

**CESEQ**



**Diplomado en Software Embebido**

Proyecto <Titulo>

DOCUMENTO: Software Development Plan #CESEQ001

Scrum Master: surname, name

Developer. surname, name

Date (YYYYMMDD): 20190405

# Log

|  |  |  |  |
| --- | --- | --- | --- |
| Version | Date (yyyymmdd) | Description | Reviewer |
| 1.0.0 | 20190405 | First release | Pérez, Adbeel |
|  |  |  |  |

# Index

Table of Contents

[1. Log 2](#_Toc14957094)

[2. Index 3](#_Toc14957095)

[3. Project Scope 4](#_Toc14957096)

[4. Deliverables 4](#_Toc14957097)

[4.1 Documents 4](#_Toc14957098)

[4.2 Code 6](#_Toc14957099)

[5. Development methodology 6](#_Toc14957100)

[6. Estimates 6](#_Toc14957101)

[7. Planning 7](#_Toc14957102)

[8. Solving Problem Strategy 7](#_Toc14957103)

[9. Design 7](#_Toc14957104)

[9.1. Standards 8](#_Toc14957105)

[9.2. Naming conventions 8](#_Toc14957106)

[10. Testing 8](#_Toc14957107)

[10.1. Verification strategy (black box test) 8](#_Toc14957108)

[10.2. White box strategy 9](#_Toc14957109)

[10.3. Cyclomatic Complexity Redundance index 9](#_Toc14957110)

[11. Release 9](#_Toc14957111)

[11.1. Integration Tests Strategy 9](#_Toc14957112)

[11.2. Validation Testing / Functional Testing 10](#_Toc14957113)

[11.3. Throughput and Flash and RAM measurement 10](#_Toc14957114)

# Project Scope

Description of the full project can be observed in the following document:

*<PROJECT\_PATH>/1) Requirements/stakeholder/20190501c Requisitos del proyecto integrador CESEQ.docx*

The project was completed with changes to the original scope specified in the aforementioned document. Those changes are listed below:

* Set Point adjustment through UART port: This project did not consider the adjustment of the Set Point using this communication protocol. Set Point is adjusted exclusively through a potentiometer.

Additionally, for those modules where the project description provided several options to proceed, the selections made by this team are listed below:

* Control Algorithm: The close-loop algorithm used for this project is of the PID type.
* Time management for processes: A scheduler was used to execute the system’s tasks.

The requirements for this project were defined in two documents:

1. *<PROJECT\_PATH>/1) Requirements/Requisitos\_ProyectoIntegrador\_DSE.pdf*
2. *<PROJECT\_PATH>/1) Requirements/Requisitos\_SW\_ProyectoIntegrador\_DSE.pdf*

The first document contains the System Requirements, while the second document contains the Software Requirements. These documents were generated with the help of an additional software, *ReqView v2.6.2*, which helped us to enumerate the requirements while they were being generated.

It should also be noted that the changes to the original scope and selections mentioned above are reflected in the requirement documents.

# Deliverables

Work products like: Code (hex), Documents (Software Requirement Document, Estimates file, Planning file, Design file, verification file, Functional testing file), or hardware if apply (schematic files, PCB file and Gerber file, general draft) **SHALL** be described here.

## 4.1 Documents

The following table contains the list of documents that will be delivered for this project. Please note that the document location is relative to the path where this document is placed (*<PROJECT\_PATH>*).

|  |  |  |
| --- | --- | --- |
| **Document Name** | **Short Description** | **Location** |
| Diagrama\_EntradasSalidas.pdf | System diagram for the project (Inputs/Outputs) |  |
| Diagrama\_Flujo.pdf | Flow chart for the code |  |
| DSE\_Gantt | Gantt Project Planning |  |
| DSE\_SW\_PI\_140619\_001 | Software diagram |  |
| Matriz\_Riesgos.xlsx | Risk Management File |  |
| Minutas.docx | Document containing dates, topics and resolution for meetings with project’s advisor. |  |
| Requisitos\_ProyectoIntegrador\_DSE.pdf | System Requirements |  |
| Requisitos\_SW\_ProyectoIntegrador\_DSE.pdf | Software Requirements |  |
| Statement Of Work.docx | Document containing details about how risks, reviews and changes were handled. |  |
| Software Design Document | Contains system and software diagrams. |  |
| Software Standards | Contains details about the software standard used for this project. |  |
| Naming Conventions | Contains details about the naming conventions used inside the code. |  |
| Blackbox Test Baseline | Details Blackbox strategy. |  |
| Whitebox Test Baseline | Details Whitebox strategy. |  |
| Integration Test Baseline | Details Integration testing strategy. |  |
| Validation Test Baseline | Details Validation strategy. |  |
| ThroughputFlashRAM Test Procedure | Details test procedures and results for the throughput, Flash and RAM measurements. |  |
| Blackbox Test Results | Blackbox Test Results |  |
| Whitebox Test Results | Whitebox Test Results |  |
| Integration Test Results | Integration Test Results |  |
| Validation Test Results | Validation Test Results |  |
| Auditoria de calidad V1.0.docx | Format for the Project’s evaluation |  |

## 4.2 Code

The complete RENESAS project can be found in the following zip file:

*<PROJECT\_PATH>/3) Design/DSE\_Project.zip*

Although several files are contained inside the RENESAS project, only those manually modified are listed in the table below. Please note that the files location is relative to the zip file *(<PROJECT\_PATH>/3) Design/DSE\_Project.zip*).

|  |  |  |
| --- | --- | --- |
| **File Name** | **Short Description** | **Location** |
| guiapp\_event\_handlers.c | Event handlers for actions related to the LCD display | src/ |
| main\_thread\_entry.c | Main function. Timers, Interruptions, PWM are initialized. | src/ |
| common.h | Name definitions used throughout the RENESAS project. | src/ |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |

# Development methodology

In case the team select SCRUM Methodology, it **SHALL** specify the controls like:

* Scrum board,
* Length of the sprint.
* Schedule of the Meetings.
* Positions: Scrum masters, product owner and developers.
* Planning board.

# Estimates

* Estimates **SHALL** contain all the Inputs, like:
  + Facts:
    - Board availabilty
    - Plant availability
    - PC availability
    - Osciloscope
    - Signal generator
    - Multimeter
    - Power supply
    - Human resources
      * Product owner should be the tutor
      * Master scrum and developer (better called as leader)
      * Developer
  + Assumptions:
    - Laboratory time availability.
    - Team time availability.
    - Hardware in good conditions.
* It **SHALL** be defined all risk, remember that this is an input for the DFMEA:
  + - Hardware damaged.
    - Team is not complete due other projects or trips.
    - UTEQ holidays.
    - New hardware and microcontroller
    - Programming language, SW IDE or Hw platform unkown.
    - SW Module unknown.
    - Error HW configuration.
    - OS unkown.
    - Error in the OS Configuration.
    - Error hardware connection.
    - etc
* It **SHALL** have a breakdown of all task and activities that are needed and analyze their dependency between them, some good examples to estimate are:
  + **Hardware modules** (devices like pc, debugger, board, plant, etc).
  + **Software** **Modules** (RAM, ROM and throughput)
    - Time estimated for each Modules development, it means, they need to reflect the time for every task needed to implement each module like: (UART, I2C or SPI, ADC, PWM, HMI, PID Algorithm implementation, Operative system implementation, etc).
  + **Create and update documents** (design planning verification and so on). Consider the time to create and update documents (SDP, schedule, control code, meetings and peer reviews).
  + **Create, update and execute Verification** **Plan** (white and black test, cyclomatic complexity index calculation, Integration testing, throughput, RAM and FLASH measurement, C99, C11 or other standard evaluation).

# Planning

* It **SHALL** contain the roll definitions of the team members and their responsibilities.
* All the tasks from estimates section **SHALL** be reflected into the Schedule and assigned to the team. Every task **SHALL** contain the definition of done.
* Remember that any document created, updated, White/Black test execution, Integration testing execution, meetings etc, **SHALL** be contained in this section as part of the activities of the plan.

This section **MUST** be contained in this document or in a different document linked to this section, the new document SHALL be contained at:

<PROJECT\_PATH>\2) Planning\7. Planning\_20190405.xlsx

# Solving Problem Strategy

* This section SHALL contain an FMEA for the full Project considering the sw functionalities defined in the risk analysis from the estimates section.
* In case an error be detected during the development stage, this section SHALL contain a mitigation plan including the 5 whys methodology for hw, sw and document issues.

This section MUST be contained in this document or in a different document linked to this section, the new document SHALL be contained at:

<PROJECT\_PATH>\2) Planning\8. DFMEA\_20190405.xlsx

# Design

This section **SHALL** contain Static and dynamic modeling diagrams like: block diagram flow diagram, call tree diagram, state machine diagram, sequence diagram and others depending on the programming paradigm.

Additionally, this section SHALL contain control diagram where is defined the: inputs, outputs, noise, and its feedback (if apply).

This section MUST be contained in this document or in a different document linked to this section, the new document SHALL be contained at:

<PROJECT\_PATH>\3) Design\9. SoftwareDesignDocument\_20190405.docx

Sections 9.1. and 9.2. MUST be contained in this document or MUST be divided into different documents. With the naming defined in every section.

## Standards

In case C89-C90, C11 or other standard be used, it SHALL be specified in this section and additionally add the link to the standard used.

Additionally, the tool used to evaluate the standard SHALL be defined here if apply.

This section MUST be contained in this document or in a different document linked to this section, the new document SHALL be contained at:

<PROJECT\_PATH>\3) Design\ 9.1. SoftwareStandards\_20190405.docx

## Naming conventions

The tags SHALL be defined for: local and global variables, local and global functions, macros, enumerations and structures.

It is **SUGGESTED** to use capital letter for global variables and macros.

In case prefix be used, it is SUGGESTED to consider for variable type, module or file, for example:

uint8\_var1

adc\_variable1

etc.

File names SHALL have a convention defined in this section, for instance: first letter SHALL be capital.

For folder in code, it SHALL be defined the names or conventions used.

This section MUST be contained in this document or in a different document linked to this section, the new document SHALL be contained at:

<PROJECT\_PATH>\3) Design\9.2. NamingConventions\_20190405.docx

In code comments, It SHALL contain the requirements which is implemented with the code described.

# Testing

## Verification strategy (black box test)

This section SHALL be contained at:

<PROJECT\_PATH>\4) Verification\10.1. BlackboxTest\_baseline.docx

…and its results SHALL be located with the date as suffix, as following is indicated:

<PROJECT\_PATH>\4) Verification\Results\10.1. BlackboxTest\_20190405.docx

Every time a module or feature is implemented, it SHALL contain their tests section and SHALL be contained with the reference to the requirement number in order to have traceability.

## White box strategy

It SHALL define the software which is going to be used, for instance: gtest, junit, sunit, etc.

A document baseline SHALL be created as a reference for all the project implementation. This document SHALL be located at:

<PROJECT\_PATH>\4) Verification\10.2. WhiteboxTest\_baseline.docx

…and its result SHALL be located at:

<PROJECT\_PATH>\4) Verification\Results\10.2. WhiteboxTest\_20190405.docx

Every time a module or feature is implemented, every test case SHALL contain a reference to the requirement number in order to have traceability.

## Cyclomatic Complexity Redundance index

<This section is optional>

This section MUST be contained in this document or in a different document linked to this section, the new document SHALL be contained at:

<PROJECT\_PATH>\4) Verification\ 10.3. CCRI\_20190405.docx

…in case this section is implemented, then its result SHALL be located at:

<PROJECT\_PATH>\4) Verification\Results\10.3. CCRI\_20190405.docx

# Release

Firmware version number SHALL be defined in this section, and the strategy used for that, an example MUST be:

Date/Hw version/Sw version

20190405/001/ 001

## Integration Tests Strategy

This section SHALL be contained in the planning and reflected in the schedule.

IT **SHALL** be defined a document baseline as a reference for all the project implementation. This document **SHALL** be located at:

<PROJECT\_PATH>\4) Verification\11.1. IntegrationTesting\_baseline.docx

…and its RESULT SHALL be located at:

<PROJECT\_PATH>\4) Verification\Results\11.1. IntegrationTesting\_20190405.docx

Every time a module or feature is implemented, every test case SHALL contain a reference to the requirement number in order to have traceability.

This test MUST contain the plant connected or not.

## Validation Testing / Functional Testing

This section SHALL be contained in the planning and reflected in the schedule.

IT **SHALL** be defined a document baseline as a reference for all the project implementation. This document **SHALL** be located at:

<PROJECT\_PATH>\4) Verification\11.2. ValidationTesting\_baseline.docx

…and its RESULT SHALL be located at:

<PROJECT\_PATH>\4) Verification\Results\11.2. ValidationTesting\_20190405.docx

Every time a module or feature is implemented, every test case SHALL contain a reference to the requirement number in order to have traceability.

This test SHALL contain the plant connected.

## Throughput and Flash and RAM measurement

This section SHALL be contained in the planning and reflected in the schedule.

It SHALL define the RAM, Flash and Throughtput measurements strategy at:

<PROJECT\_PATH>\4) Verification\ 11.3. ThroughputRAMFlash\_procedure