**UNIVERSIDAD TECNOLÓGICA DE QUERÉTARO**

**CESEQ**



**Diplomado en Software Embebido**

Proyecto <Titulo>

DOCUMENTO: Software Development Plan #CESEQ001

Scrum Master: surname, name

Developer. surname, name

Date (YYYYMMDD): 20190405

# Log

|  |  |  |  |
| --- | --- | --- | --- |
| Version | Date (yyyymmdd) | Description | Reviewer |
| 1.0.0 | 20190405 | First release | Pérez, Adbeel |
|  |  |  |  |

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# Project Scope

Description of the full project can be observed in the following document:

*<PROJECT\_PATH>/1) Requirements/stakeholder/20190501c Requisitos del proyecto integrador CESEQ.docx*

The project was completed with changes to the original scope specified in the aforementioned document. Those changes are listed below:

* Set Point adjustment through UART port: This project did not consider the adjustment of the Set Point using this communication protocol. Set Point is adjusted exclusively through a potentiometer.

Additionally, for those modules where the project description provided several options to proceed, the selections made by this team are listed below:

* Control Algorithm: The close-loop algorithm used for this project is of the PID type.
* Time management for processes: A scheduler was used to execute the system’s tasks.

The requirements for this project were defined in two documents:

1. *<PROJECT\_PATH>/1) Requirements/Requisitos\_ProyectoIntegrador\_DSE.pdf*
2. *<PROJECT\_PATH>/1) Requirements/Requisitos\_SW\_ProyectoIntegrador\_DSE.pdf*

The first document contains the System Requirements, while the second document contains the Software Requirements. These documents were generated with the help of an additional software, *ReqView v2.6.2*, which helped us to enumerate the requirements while they were being generated.

It should also be noted that the changes to the original scope and selections mentioned above were done in agreement with the customer and are reflected in the requirement documents.

# Deliverables

## 4.1 Documents

The following table contains the list of documents that will be delivered for this project. Please note that the document location is relative to the path where this document is placed (*<PROJECT\_PATH>*).

|  |  |  |
| --- | --- | --- |
| **Document Name** | **Short Description** | **Location** |
| Diagrama\_EntradasSalidas.pdf | System diagram for the project (Inputs/Outputs) |  |
| Diagrama\_Flujo.pdf | Flow chart for the code |  |
| DSE\_Gantt | Gantt Project Planning |  |
| DSE\_SW\_PI\_140619\_001 | Software diagram |  |
| Matriz\_Riesgos.xlsx | Risk Management File |  |
| Minutas.docx | Document containing dates, topics and resolution for meetings with tutor. |  |
| Requisitos\_ProyectoIntegrador\_DSE.pdf | System Requirements |  |
| Requisitos\_SW\_ProyectoIntegrador\_DSE.pdf | Software Requirements |  |
| Statement Of Work.docx | Document containing details about how risks, reviews and changes were handled. |  |
| Software Design Document | Contains system and software diagrams. |  |
| Software Standards | Contains details about the software standard used for this project. |  |
| Naming Conventions | Contains details about the naming conventions used inside the code. |  |
| Blackbox Test Baseline | Details Blackbox strategy. |  |
| Whitebox Test Baseline | Details Whitebox strategy. |  |
| Integration Test Baseline | Details Integration testing strategy. |  |
| Validation Test Baseline | Details Validation strategy. |  |
| ThroughputFlashRAM Test Procedure | Details test procedures and results for the throughput, Flash and RAM measurements. |  |
| Blackbox Test Results | Blackbox Test Results |  |
| Whitebox Test Results | Whitebox Test Results |  |
| Integration Test Results | Integration Test Results |  |
| Validation Test Results | Validation Test Results |  |
| Auditoria de calidad V1.0.docx | Format for the Project’s evaluation |  |

## 4.2 Code

The complete RENESAS project can be found in the following zip file:

*<PROJECT\_PATH>/3) Design/DSE\_Project.zip*

Although several files are contained inside the RENESAS project, only those manually modified are listed in the table below. Please note that the files location is relative to the zip file *(<PROJECT\_PATH>/3) Design/DSE\_Project.zip*).

|  |  |  |
| --- | --- | --- |
| **File Name** | **Short Description** | **Location** |
| guiapp\_event\_handlers.c | Event handlers for actions related to the LCD display | src/ |
| main\_thread\_entry.c | Main function. Timers, Interruptions, PWM are initialized. | src/ |
| common.h | Name definitions used throughout the RENESAS project. | src/ |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |

# Development methodology

In case the team select SCRUM Methodology, it **SHALL** specify the controls like:

* Scrum board,
* Length of the sprint.
* Schedule of the Meetings.
* Positions: Scrum masters, product owner and developers.
* Planning board.

Mencionar sprints, juntas de cada semana con asesor, roles, encargados de épicas

# Estimates

Before making the time estimates for the activities required to complete the project, an analysis was done to identify the facts, assumptions and risks involved; this with the intention of making time estimates closer to reality, organize activities in such way that dependencies do not interfere with deliveries, and identify potential risks at early stages of the planning to be able to mitigate them with the minimum impact possible.

The facts considered for the project are the following:

* There is a workstation available with the following components:
  + PC
  + Internet connectivity
  + Oscilloscope
  + Function Generator
  + DC Power Supply
  + Multimeter
  + SK-S7G2 RENESAS Board
* The team will have a plant available with the following components:
  + Potentiometer
  + H-Bridge Motor Driver
* The following software will be available for the team to use:
  + Matlab
  + E2 Studio IDE
  + Git Hub
* Human Resources:
  + Product Owner (Tutor)
  + 2 Team Members acting as SCRUM Master and Developer

The assumptions made for the project are the following:

* Hardware is available and in good conditions.
* Software is available and has the necessary functionality to aid with the project’s deliverables.
* Laboratory will be available to work on the project on Fridays from 02:00pm to 06:00pm.
* Team members will be available to work on the project on Fridays from 02:00pm to 06:00pm.
* Project requirements will not change from those defined at the beginning of the course.

The risks identified for the project are the following:

* Unable to work with RENESAS Board outside of UTEQ
* Inaccurate planning due to lack of knowledge on project’s complexity.
* Uncalibrated sensor
* Unstable controller
* Damaged components
* Change in requirements
* Team members’ unavailability to work on project outside of Fridays

These risks were monitored throughout the development of the project using a risk matrix. This file can be found in the following path:

*<PROJECT\_PATH>/2) Planning/Matriz\_Riesgos.xlsx*

Considering all the previous points, it was possible to make estimates for the activities that needed to be done in order to complete the project. Using the SCRUM methodology, the epics and stories shown in the table below were defined. The “Estimate” column reflects the latest estimate done for the stories; these points, which represent hours, were adjusted during each Sprint.

|  |  |  |
| --- | --- | --- |
| **Activity** | **Type** | **Estimate** |
| Requirements Analysis | Epic |  |
| Read Requirements | Story | 2 |
| Requirements Definition | Story | 6 |
| Instrumentation | Epic |  |
| Hall Effect Sensor Tests | Story | 5 |
| Sensor Characterization | Story | 2 |
| Potentiometer Tests | Story | 2 |
| Potentiometer Characterization | Story | 1 |
| Display Tests | Story | 6 |
| Power | Epic |  |
| H-Driver Tests | Story | 3 |
| H-Driver Characterization | Story | 3 |
| Motor Tests | Story | 2 |
| Power Module Integration | Story | 3 |
| Controller | Epic |  |
| Control Theory Overview | Story | 3 |
| Identify Plant | Story | 2 |
| Obtain Plant’s transfer function | Story | 3 |
| Simulate plant | Story | 2 |
| Develop control algorithm | Story | 2 |
| Implement controller | Story | 5 |
| Test controller | Story | 3 |
| User Interface | Epic |  |
| Set display | Story | 3 |
| Test display | Story | 2 |
| Diagnostics | Epic |  |
| Short to Battery | Story | 3 |
| Short to Ground | Story | 3 |
| Memory corruption | Story | 2 |
| Button in short circuit | Story | 2 |
| Integration | Epic |  |
| Integration of modules | Story | 5 |
| Hardware Tests | Epic |  |
| Software Tests | Epic |  |
| Black Box Tests | Story | 6 |
| White Box Tests | Story | 6 |
| Additional Tests | Story | 2 |
| Project Management | Epic |  |
| Develop SDP | Story | 5 |
| Develop SVP | Story | 5 |
| Develop Architecture document | Story | 3 |
| Generate additional documentation | Story | 8 |

These epics and stories were saved in a GitHub repository, where the tracking was being monitored in order to analyze the progress done throughout the development of the project.

# Planning

The epics were assigned due dates in order to keep track of their progress and their estimated date of completion. This information was then placed in a Gantt chart, which was presented to the customer so he could also evaluate the progress of the project. The Gantt chart with the final plan and dates can be found in the following path:

*<PROJECT\_PATH>/2) Planning/DSE\_Gantt.pod*

The stories defined in the previous section were divided between the team members in order to be completed. The team member who was responsible of doing the necessary activities to complete the task was assigned the role of *developer*, while the other team member was assigned the role of *reviewer/tester*, who made sure the “Definition of Done” was fulfilled for that particular story.

The table below shows the developer assigned to the story as well as its definition of done, which would be used by the reviewer/tester as a parameter to validate that the story was actually complete.

|  |  |  |  |
| --- | --- | --- | --- |
| **Activity** | **Type** | **Developer** | **Definition of Done** |
| Requirements Analysis | Epic |  |  |
| Read Requirements | Story | Both | Read UTEQ’s document about project. |
| Requirements Definition | Story | Both | Upload requirements document to Github. |
| Instrumentation | Epic |  |  |
| Hall Effect Sensor Tests | Story |  | Observe in oscilloscope an error lower than 10% in measurements. |
| Sensor Characterization | Story |  |
| Potentiometer Tests | Story |  | Observe in multimeter an error lower than 10% in measurements. |
| Potentiometer Characterization | Story |  |
| Display Tests | Story |  | Upload project with customized display to Github. |
| Power | Epic |  |  |
| H-Driver Tests | Story |  | Pass (whitebox/blackbox/ integration/validation) tests |
| H-Driver Characterization | Story |  |
| Motor Tests | Story |  | Pass (whitebox/blackbox/ integration/validation) tests |
| Power Module Integration | Story |  |
| Controller | Epic |  |  |
| Control Theory Overview | Story |  | Identify possible controller types to use. |
| Identify Plant | Story |  | Generate control diagram. |
| Obtain Plant’s transfer function | Story |  | Document transfer function in requirements. |
| Simulate plant | Story |  | Generate plots in Matlab. |
| Develop control algorithm | Story |  | Upload code to Github. |
| Implement controller | Story |  | Integrate controller code. |
| Test controller | Story |  | Pass (whitebox/blackbox/ integration/validation) tests |
| User Interface | Epic |  |  |
| Set display | Story |  | Configure display information according to requirements. |
| Test display | Story |  | Integrate display code. |
| Diagnostics | Epic |  |  |
| Short to Battery | Story |  | Pass (whitebox/blackbox/ integration/validation) tests |
| Short to Ground | Story |  | Pass (whitebox/blackbox/ integration/validation) tests |
| Memory corruption | Story |  | Pass (whitebox/blackbox/ integration/validation) tests |
| Button in short circuit | Story |  | Pass (whitebox/blackbox/ integration/validation) tests |
| Integration | Epic |  |  |
| Integration of modules | Story |  | Pass (whitebox/blackbox/ integration/validation) tests |
| Hardware Tests | Epic |  |  |
| Software Tests | Epic |  |  |
| Black Box Tests | Story |  | Generate Black Box Results document. |
| White Box Tests | Story |  | Generate White Box Results document. |
| Additional Tests | Story |  | Generate Additional Tests document. |
| Project Management | Epic |  |  |
| Develop SDP | Story |  | Complete SDP has been uploaded to Github. |
| Develop SVP | Story |  | Complete SVP has been uploaded to Github. |
| Develop Architecture document | Story |  | Architecture document has been uploaded to Github. |
| Generate additional documentation | Story |  | Additional documentation has been uploaded to Github following folder structure. |

# Solving Problem Strategy

For the Problem Solving Strategy to be used, FMEA was discussed with the customer and it was determined that it will not be used for this project since it is more oriented to systems; for software projects, risks can be monitored through a risk matrix, where the occurrence and criticality/impact can be determined for every risk that has been identified. The risk matrix used for this project can be found in the following file:

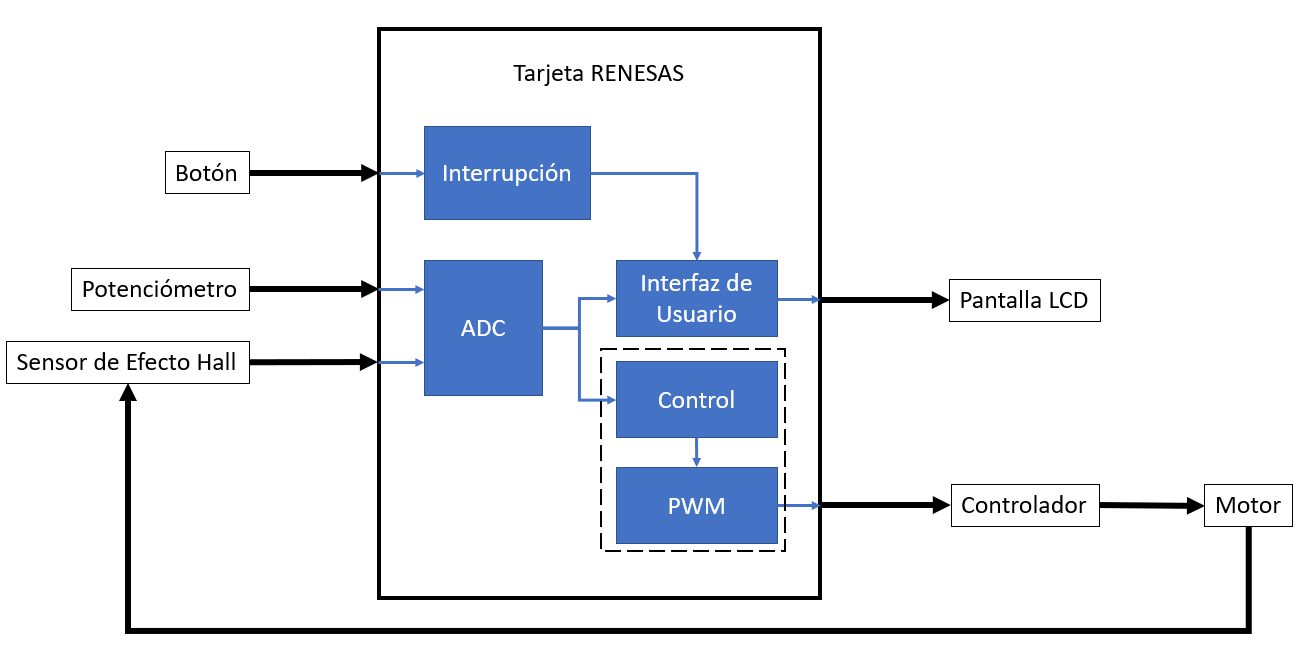
*<PROJECT\_PATH>/2) Planning/Matriz\_Riesgos.xlsx*

Placeholder for additional section details

# Design

## System Diagram

The System Diagram below identifies the inputs and outputs of the system based on the project’s requirements (image in Spanish).

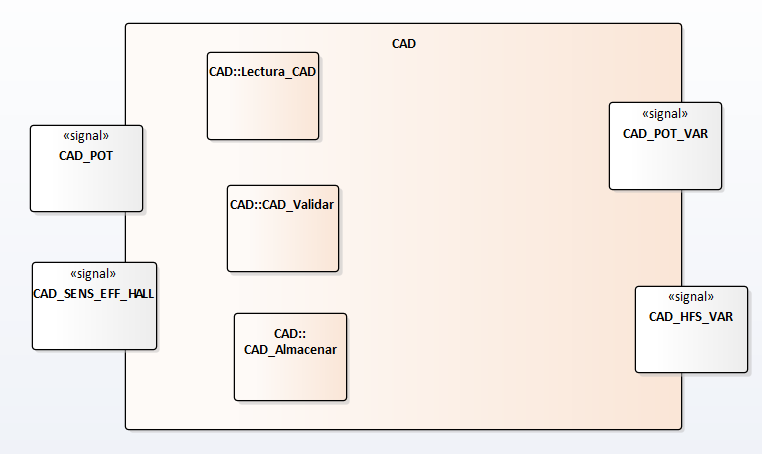


## Software Diagram

To develop the Software Diagram, the *Enterprise Architect v13.5.1351* software was used to identify the modules that would have to be implemented, including their functions, inputs and outputs.

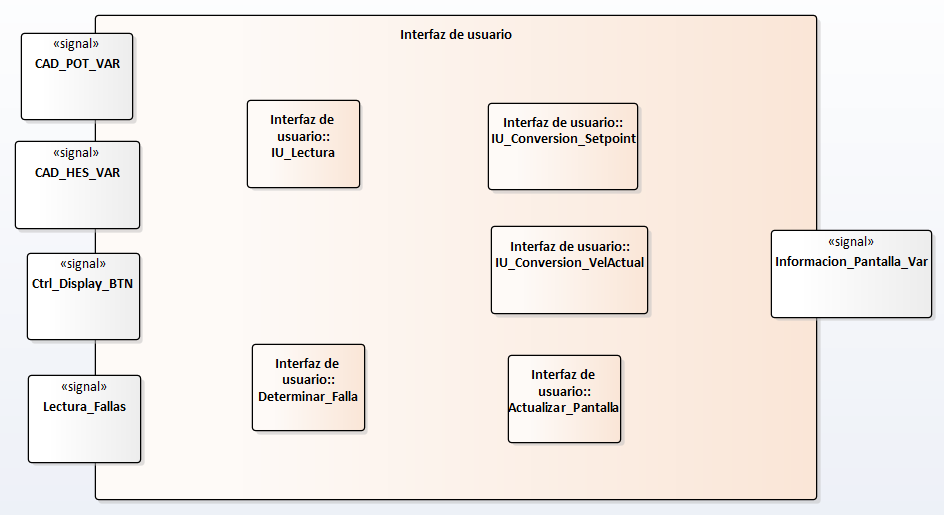
### ADC

For the ADC module, two inputs were considered, one coming from the potentiometer and another one from the Hall Effect Sensor. This module contains three functions, one to read the incoming ADC value, another one to validate the reading and finally one to store the value in its corresponding variable, which could be either POT\_VAR or HFS\_VAR, the outputs of the module.



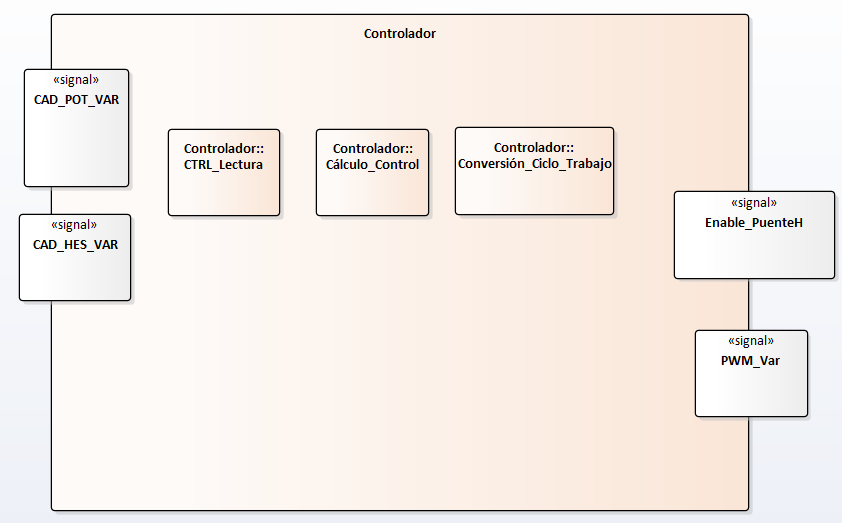
### User Interface

For the User Interface module, its inputs will be the outputs from the ADC module together with the button status that will change the menu shown in the display and the information from the diagnostics. This module will read the inputs and, depending on the menu being displayed, will either convert the ADC and Sensor’s value to the set point and speed respectively or will determine if the monitored values lead to a short to battery or short to ground. Finally, one last function will be in charge of displaying the appropriate message on the display.



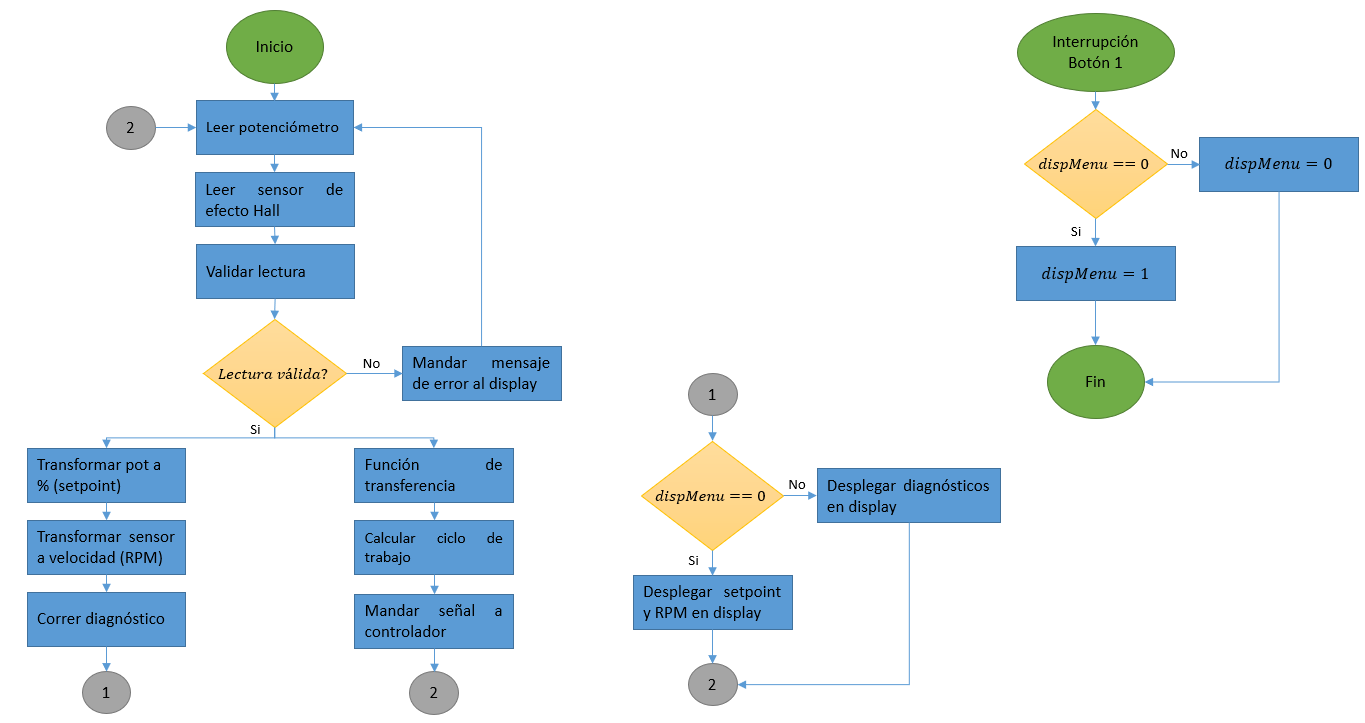
### Controller

For the Controller module, the outputs from the ADC (which have already been validated) will be the inputs. These signals will be read, then they will be used for the control algorithm in order to define the new speed that must be set for the motor and finally that speed will be converted to a duty cycle that will be assigned to the RENESAS output set as PWM.



## Flow Diagram

The flow diagram below shows what the program will do throughout its execution. First, it will read and validate information coming from the potentiometer and the Hall Effect sensor, then it will do several tasks: calculate the set point, calculate the actual speed, run the diagnostics, run the controller algorithm, and calculate the new duty cycle; then it will send this signal to the power driver. A digital button configured on the display will trigger an interruption that will toggle between the two available menus, either the main menu (showing speed, duty cycle, etc.) or the diagnostics menu.



## Control Diagram

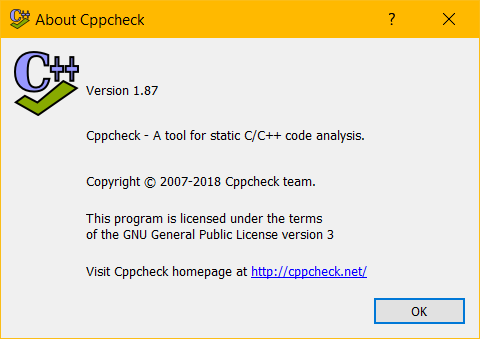
PENDING. Add control diagram and description.

## Standards

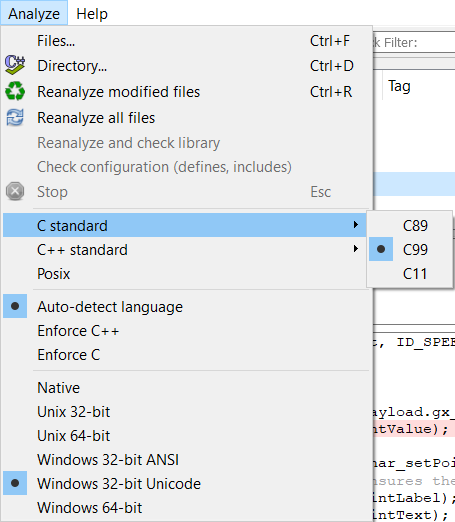
The coding standard used for this project was **C99**, formally known as ISO/IEC 9899:2018. There is no direct link to view this standard, since the ANSI WEBSTORE charges for the ability to download a PDF copy of the document. Instead, the link to the download page is shown below:

<https://webstore.ansi.org/Standards/ISO/ISOIEC98992018>

In order to validate that the standard was followed correctly, an additional software tool was used, *Cppcheck v1.87*:



This program allows users to analyze C code files with a specific standard from its catalogue; in this case, C99 was selected:



All errors or warnings shown by the tool were corrected before delivering the final version of the code.

## Naming conventions

The tags SHALL be defined for: local and global variables, local and global functions, macros, enumerations and structures.

It is **SUGGESTED** to use capital letter for global variables and macros.

In case prefix be used, it is SUGGESTED to consider for variable type, module or file, for example:

uint8\_var1

adc\_variable1

etc.

File names SHALL have a convention defined in this section, for instance: first letter SHALL be capital.

For folder in code, it SHALL be defined the names or conventions used.

This section MUST be contained in this document or in a different document linked to this section, the new document SHALL be contained at:

<PROJECT\_PATH>\3) Design\9.2. NamingConventions\_20190405.docx

In code comments, It SHALL contain the requirements which is implemented with the code described.

# Testing

## Verification strategy (black box test)

This section SHALL be contained at:

<PROJECT\_PATH>\4) Verification\10.1. BlackboxTest\_baseline.docx

…and its results SHALL be located with the date as suffix, as following is indicated:

<PROJECT\_PATH>\4) Verification\Results\10.1. BlackboxTest\_20190405.docx

Every time a module or feature is implemented, it SHALL contain their tests section and SHALL be contained with the reference to the requirement number in order to have traceability.

## White box strategy

It SHALL define the software which is going to be used, for instance: gtest, junit, sunit, etc.

A document baseline SHALL be created as a reference for all the project implementation. This document SHALL be located at:

<PROJECT\_PATH>\4) Verification\10.2. WhiteboxTest\_baseline.docx

…and its result SHALL be located at:

<PROJECT\_PATH>\4) Verification\Results\10.2. WhiteboxTest\_20190405.docx

Every time a module or feature is implemented, every test case SHALL contain a reference to the requirement number in order to have traceability.

## Cyclomatic Complexity Redundance index

<This section is optional>

This section MUST be contained in this document or in a different document linked to this section, the new document SHALL be contained at:

<PROJECT\_PATH>\4) Verification\ 10.3. CCRI\_20190405.docx

…in case this section is implemented, then its result SHALL be located at:

<PROJECT\_PATH>\4) Verification\Results\10.3. CCRI\_20190405.docx

# Release

Firmware version number SHALL be defined in this section, and the strategy used for that, an example MUST be:

Date/Hw version/Sw version

20190405/001/ 001

## Integration Tests Strategy

This section SHALL be contained in the planning and reflected in the schedule.

IT **SHALL** be defined a document baseline as a reference for all the project implementation. This document **SHALL** be located at:

<PROJECT\_PATH>\4) Verification\11.1. IntegrationTesting\_baseline.docx

…and its RESULT SHALL be located at:

<PROJECT\_PATH>\4) Verification\Results\11.1. IntegrationTesting\_20190405.docx

Every time a module or feature is implemented, every test case SHALL contain a reference to the requirement number in order to have traceability.

This test MUST contain the plant connected or not.

## Validation Testing / Functional Testing

This section SHALL be contained in the planning and reflected in the schedule.

IT **SHALL** be defined a document baseline as a reference for all the project implementation. This document **SHALL** be located at:

<PROJECT\_PATH>\4) Verification\11.2. ValidationTesting\_baseline.docx

…and its RESULT SHALL be located at:

<PROJECT\_PATH>\4) Verification\Results\11.2. ValidationTesting\_20190405.docx

Every time a module or feature is implemented, every test case SHALL contain a reference to the requirement number in order to have traceability.

This test SHALL contain the plant connected.

## Throughput and Flash and RAM measurement

This section SHALL be contained in the planning and reflected in the schedule.

It SHALL define the RAM, Flash and Throughtput measurements strategy at:

<PROJECT\_PATH>\4) Verification\ 11.3. ThroughputRAMFlash\_procedure